What is claimed is:

Sub A1

1. A voltage divider system (102), comprising:

a high voltage impedance element (104), connected to an input node for receiving an input signal;

a low voltage impedance element (106), connected to the high voltage impedance element (104); and

at least one guard element (118), the at least one guard element (118) being coupled between the high voltage impedance element (104) and ground.

2. The system of claim 1, further comprising a sample node (110) between the high voltage impedance element (104) and the low voltage impedance element (106) for sampling a -reduced voltage representation of the input signal.

3. The system of claim 2, wherein the sample node (110) is connected to a measurement device (116) to perform the sampling.

4. The system of claim 3, wherein the measurement device (116) samples at least one of voltage, current, frequency, and phase.

5. The system of claim 1, wherein the high voltage impedance element (104) comprises at least one resistive element.

6. The system of claim 5, wherein the at least one resistive element comprises at least one resistor.

7. The system of claim 6, wherein the at least one resistor comprises a plurality of resistors.

8. The system of claim 1, wherein the at least one guard element (118) comprises at least one capacitive element.

Sub A2

9. The system of claim 8, wherein the at least one capacitive element comprises at least one capacitor.

10. The system of claim 9, wherein the at least one capacitor comprises a plurality of capacitors.

11. The system of claim 1, wherein the at least one guard element (118) comprises at least two guard elements.

12. The system of claim 10, wherein the at least two guard element (118)s comprise three or more guard elements.

13. The system of claim 8, wherein the at least one guard element (118) further comprises at least one resistive guard element (124) coupled to the at least one capacitive element.

Sub A3

14. The system of claim 13, wherein the at least one resistive guard element (124) comprises at least one resistor coupled to the at least one capacitive element.

15. The system of claim 13, wherein the at least one resistive guard element (124) increases a stability of a voltage drop across the high voltage impedance element (104).

16. The system of claim 1, wherein the at least one guard element (118) is coaxially mounted around the high voltage impedance element (104).

17. The system of claim 1, wherein the at least one guard element (118) shunts stray capacitive currents to ground.

18. The system of claim 17, wherein the shunted stray capacitive currents stabilize a frequency response of the voltage divider (102).

Sub A4

19. A method for processing a signal, comprising:

a) receiving an input signal via an input node (108) connected to a high voltage impedance element (104);

b) communicating a reduced voltage representation of the input signal from the high voltage impedance element (104) to a low voltage impedance element (106); and

c) coupling at least one guard element (118) between the high voltage impedance element (104) and ground.

20. The method of claim 19, further comprising a step of d) sampling the reduced voltage representation of the input signal at a sample node (110) between the high voltage impedance element (104) and the low voltage impedance element (106).

21. The method of claim 20, further comprising a step of e) connecting a measurement device (116) to the sample node (110) to perform the sampling.

22. The method of claim 21, further comprising a step of f) sampling at least one of voltage, current, frequency, and phase in the measurement device (116).

23. The method of claim 19, wherein the high voltage impedance element (104) comprises at least one resistive element.

24. The method of claim 23, wherein the at least one resistive element comprises at least one resistor.

25. The method of claim 24, wherein the at least one resistor comprises a plurality of resistors.

26. The method of claim 19, wherein the guard element (118) comprises at least one capacitive element.

Sub A5) 27. The method of claim 26, wherein the at least one capacitive element comprises at least one capacitor.

28. The method of claim 27, wherein the at least one capacitor comprises a plurality of capacitors.

29. The method of claim 19, wherein the at least one guard element (118) comprises at least two guard elements.

30. The method of claim 29 wherein the at least two guard element (118)s comprise three or more guard elements.

31. The method of claim 26, wherein the at least one guard element (118) further comprises at least one resistive guard element (124), further comprising a step of g) coupling the at least one resistive guard element (124) to the at least one capacitive element.

Sub A6) 32. The method of claim 31, wherein the at least one resistive guard element (124) comprises at least one resistor coupled to the at least one capacitive element.

33. The method of claim 32, wherein the at least one resistive guard element (124) increases a stability of a voltage drop across the high voltage impedance element (104).

34. The method of claim 19, wherein the at least one guard element (118) is coaxially mounted around the high voltage impedance element (104).

35. The method of claim 19, further comprising a step of h) shunting stray capacitive currents to ground via the at least one guard element (118).

36. The method of claim 35, wherein the shunted stray capacitive currents stabilize a frequency response.

Sub A7) 37. A voltage divider system, comprising:

high voltage impedance means (104), connected to an input node for receiving an input signal;

low voltage impedance means (106), connected to the high voltage impedance means (104); and

at least one guard means (118), the at least one guard means (118) being coupled between the high voltage impedance means (104) and ground.

38. The system of claim 37, further comprising a sample node (110) between the high voltage impedance means (104) and the low voltage impedance means (106) for sampling a -reduced voltage representation of the input signal.

39. The system of claim 38, wherein the sample node (110) is connected to a measurement means (116) to perform the sampling.

40. The system of claim 39, wherein the measurement means (116) samples at least one of voltage, current, frequency, and phase.

41. The system of claim 37, wherein the high voltage impedance means (104) comprises at least one resistive element.

42. The system of claim 41, wherein the at least one resistive element comprises at least one resistor.

43. The system of claim 42, wherein the at least one resistor comprises a plurality of resistors.

44. The system of claim 37, wherein the at least one guard means (118) comprises at least one capacitive element.

45. The system of claim 34, wherein the at least one capacitive element comprises at least one capacitor.

46. The system of claim 45, wherein the at least one capacitor comprises a plurality of capacitors.

47. The system of claim 37, wherein the at least one guard means (118) comprises at least two guard means.

48. The system of claim 47, wherein the at least two guard means comprise three or more guard means.

49. The system of claim 37, wherein the at least one guard means (118) further comprises at least one resistive guard means (124) coupled to the at least one capacitive means.

50. The system of claim 49, wherein the at least one resistive guard means comprises at least one resistor coupled to the at least one capacitive means.

51. The system of claim 49, wherein the at least one resistive guard means (124) increases a stability of a voltage drop across the high voltage impedance element (104).

52. The system of claim 37, wherein the at least one guard means (118) is coaxially mounted around the high voltage impedance means (104).

53. The system of claim 37, wherein the at least one guard means (118) shunts stray capacitive currents to ground.

54. The system of claim 53, wherein the shunted stray capacitive currents stabilize a frequency response of the voltage divider (102).

Sub A10

55. A voltage divider (102), comprising:

a plurality of series-connected high voltage resistors (114a, 114b ... 114n), the series-connected high voltage resistors (114a, 114b ... 114n) connected to an input node (110) for receiving an input signal;

at least one low voltage resistive element (106), the at least one low voltage resistive element (106) connected to the series-connected high voltage resistors (114a, 114b ... 114n); and

at least one capacitive guard (118), the at least one capacitive guard (118) connected between the series-connected high voltage resistors (114a, 114b ... 114n) and ground.

56. The voltage divider of claim 55, wherein the at least one capacitive guard (118) comprises a plurality of capacitors.

57. The voltage divider of claim 55, wherein the at least one capacitive guard (118) comprises at least two capacitive guards.

58. The voltage divider of claim 57, wherein the at least two capacitive guards comprise three or more capacitive guards.

59. The voltage divider of claim 55, wherein the at least one capacitive guard (118) further comprises at least one resistive guard (124) coupled to the at least one capacitive guard (118).

Sub A11

60. The voltage divider of claim 59, wherein the at least one resistive guard (124) comprises at least one resistor coupled to the at least one capacitive guard (118).

61. The voltage divider of claim 59, wherein the at least one resistive guard (124) increases a stability of a voltage drop across the series-connected high voltage resistors (114a, 114b ... 114n).

62. The voltage divider of claim 55, wherein the at least one capacitive guard (118) shunts stray capacitive current to ground.

63. The voltage divider of claim 62, wherein the shunted stray capacitive currents stabilize a frequency response of the voltage divider (102).

Add A12